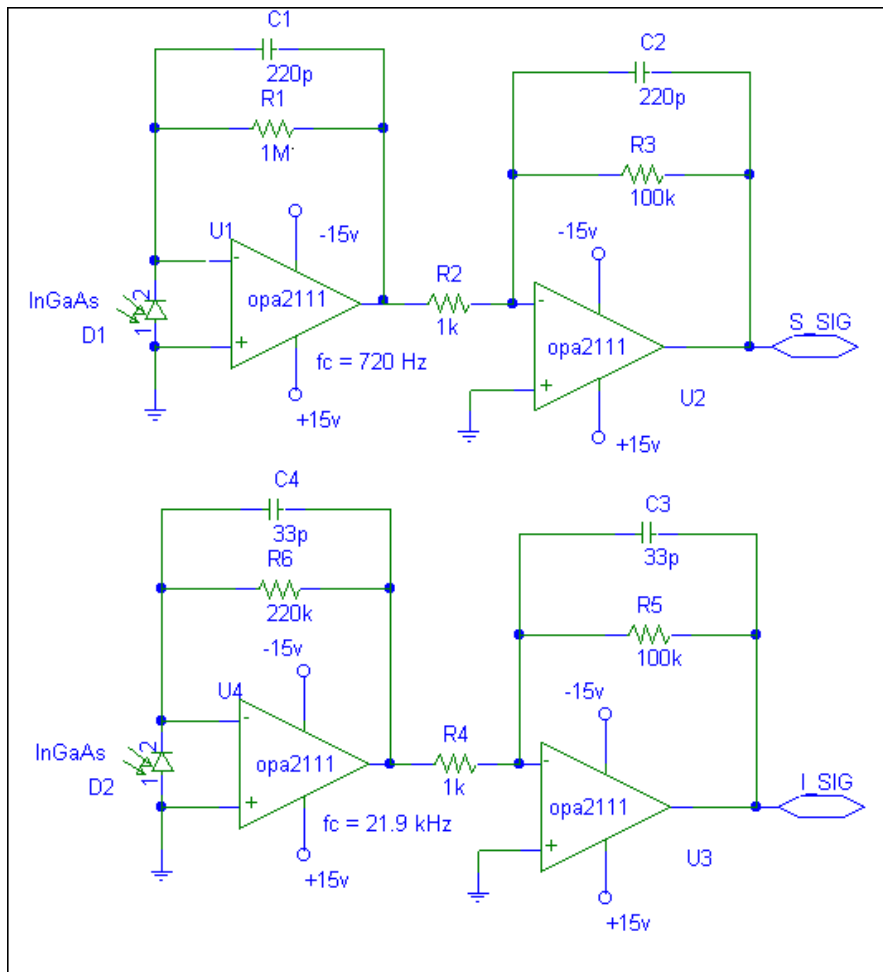


## **NOTICE**

This Appendix contains information that was left out of the original dissertation document at the request of the author and advisor. This information is presented here for members of the WPI Community only and should not be distributed to the general public.

## APPENDIX: HARDWARE

The circuit gain is actually produced in two stages, in order to reduce the chance of oscillation. Ultra-high precision, ultra-low noise, and ultra-low distortion operational amplifiers were required for this application, due to the extremely small signal that is produced by the photodetectors. An OPA-2111 (Burr-Brown) was chosen. This dual FET (field effect transistor) op-amp meets the precision, noise, and distortion requirements of this application. The dual packaging allows us to keep the detector circuitry small in size. Figure A.1 is a circuit diagram of the detector board.



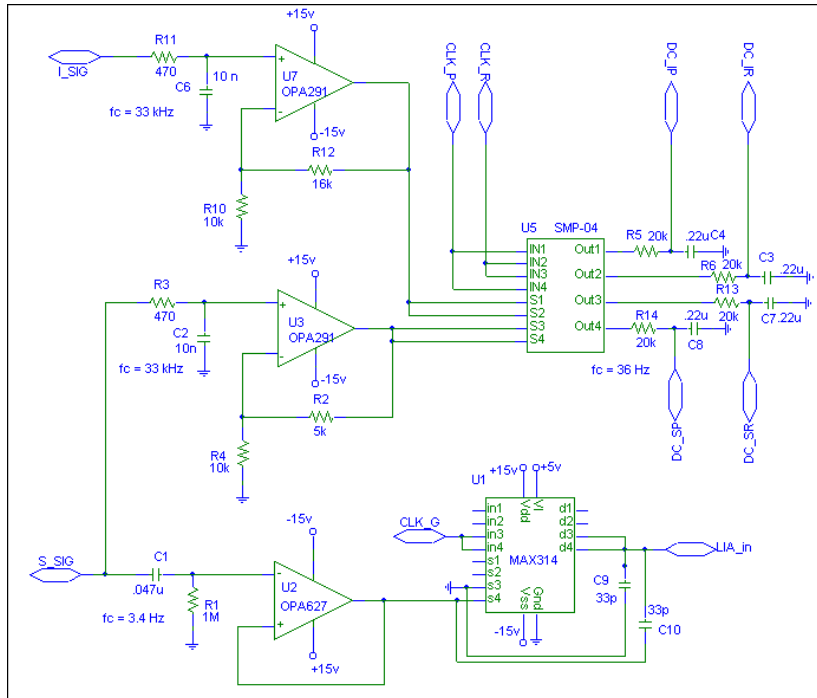
**Figure A.1: The Input Light Detector and Sample Light Detector amplifier circuits. *S\_SIG* is the amplified signal coming from the Sample Light Detector, and *I\_SIG* is the amplified signal coming from the Input Light Detector.**

The first stage is a current to voltage converter. The InGaAs detector supplies a current proportional to the number of photons that hit it. For the SLD, the gain of this first stage is  $-1.0 \cdot 10^6$  V/A. The second stage is an inverting amplifier with a gain of  $-100$ , for an overall gain of  $1.0 \cdot 10^8$  V/A. Both stages have a 220 pF filtering capacitor in the feedback loop to reduce electrical noise. The cutoff frequency for this circuit is 720 Hz.

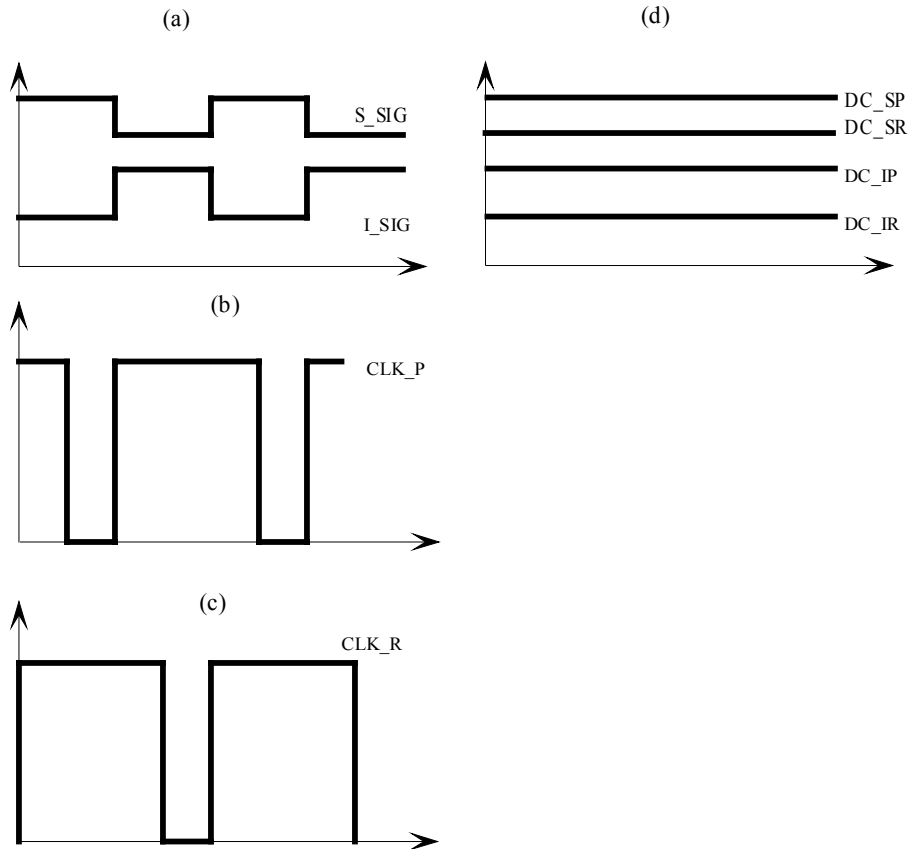
The output of the SLD amplifier circuit is known as **S\_SIG**, and the output of the ILD amplifier circuit is known as **I\_SIG**. For the ILD, the first stage gain is  $-2.2 \cdot 10^5$  V/A, and the second stage gain is  $-100$ , for an overall gain of  $2.2 \cdot 10^7$  V/A. The cutoff frequency for the ILD is 21.9 kHz.

#### *A.1.1.1 Signal Demodulator*

Once the two light signals have been transduced into electrical signals (**I\_SIG** and **S\_SIG**), and amplified by the two-stage amplifier, it is necessary to separate each phase of the signals based on the active wavelength. In Figure A.2, the circuitry required to perform this function is shown. In the top part of the figure, the signals **I\_SIG** and **S\_SIG** are both passed through low pass filters ( $f_c = 33$  kHz), and given gains of 2.6 and 1.5, respectively. The two signals are then sent to an SMP-04 (PMI) Sample and Hold module. This IC (Integrated Circuit) provides four separate sample and hold circuits, each with their own input signal. Two of these inputs are connected to the Principal wavelength gating signal **CLK\_P**, and the other two are connected to the Reference wavelength gating signal **CLK\_R**. These signals have an active-low duty cycle of 25%. **CLK\_P** is active during the last half of the Principal wavelength portion of the cycle. **CLK\_R** is active during the last half of the Reference wavelength portion of the cycle. The duty cycle for these waveforms is 25% rather than 50% to account for the transients that occur when the wavelengths are switched. See Figure A.3. The signal inputs are **I\_SIG** and **S\_SIG**, which have been amplified and filtered as stated above. The outputs of the SMP-04 are four DC signals. Signal **S\_SIG** is separated into two signals: **DCSP** and **DCSR**. **DCSP** corresponds to the value of **S\_SIG** during the period of time when the Principal wavelength is active, while **DCSR** corresponds to the value of **S\_SIG** during the period of time when the Reference wavelength is active. **I\_SIG** is similarly separated into **DCIP** and **DCIR**. These four signals are low passed filtered ( $f_c=36$  Hz). This separation is illustrated in Figure A.3. The lower portion of Figure A.2 is a gating circuit that is necessary to remove the large transients that are produced by the switching of wavelengths. This portion of the circuit prepares **S\_SIG** to enter the Lock In Amplifier (LIA), which performs the differential comparison between **S\_SIG** amplitudes at the two wavelength phases. The signal **CLK\_G** has a frequency twice that of the wavelength switching frequency **CLK\_REF**. It is applied to an analog switch (MAX313, Maxim), and the first half of each cycle is gated out. In addition to transient gating, the signal also passes through a high pass filter. This is because the signal must be AC-coupled into the LIA. The signals **CLK\_P** and **CLK\_R** have a 25% low duty cycle,



**Figure A.2:** The signals **S\_SIG** and **I\_SIG** are demodulated into two separate signals, one for each phase of the light signal. **S\_SIG** is also gated in order to suppress the large transient signals that result from the switching of wavelengths.

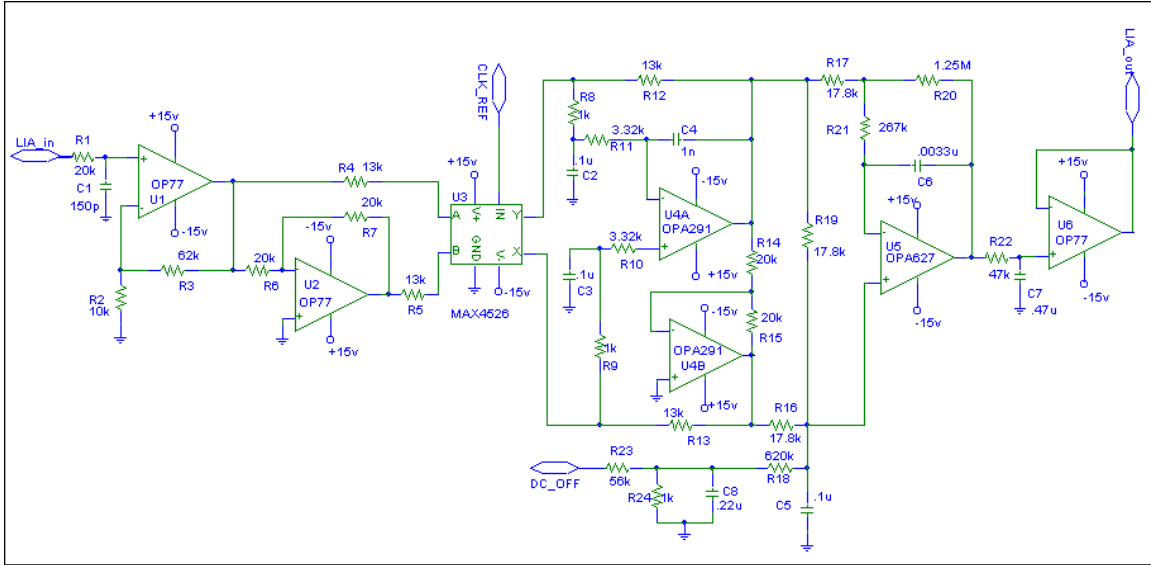


*Figure A.3: S\_SIG and I\_SIG are demodulated into four separate DC signals by the signals CLK\_P and CLK\_R. In (a), the input signals are shown. In (b), the output signals are shown. Figures (c) and (d) show the clocking signals CLK\_P and CLK\_R.*

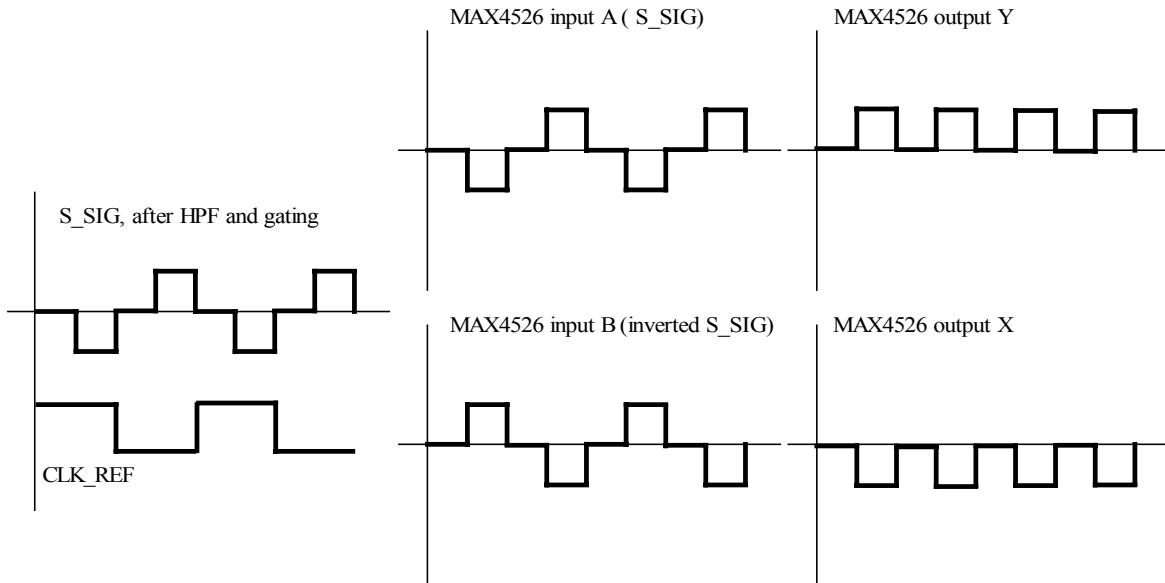
#### A.1.1.2 Lock in Amplifier

The lock in amplifier module is used to extract the signal from S\_SIG. The electrical diagram of this sub-module is shown in Figure A.5. The input to this circuit is the transient-gated, high pass filtered signal that originated at the SLD. The high pass filter is necessary so that the signal can be AC coupled into the lock in amplifier. This is necessary to remove the DC component of the signal. This signal is then low pass filtered ( $f_c=53$  kHz), and given a gain of approximately 7. The signal then splits into two different paths. In the top path, the signal remains unchanged. In the bottom path, it is inverted. It then passes to an analog switch, the MAX4526 (Maxim). The switch is toggled by the CLK\_REF signal. During the “on” part of the CLK\_REF cycle, the Y output of the MAX4526 is connected to the non-inverted signal that is on the A input. During the other part of the cycle, the Y output is connected to the inverted signal that is present on the B input. The X output is connected to the other signal. This has the effect of putting the positive portion of the signal always on the Y output and the negative portion of the signal on the X input. This process is illustrated in Figure A.4. Now that the signal has been separated into positive and negative portions, it is put into a current summing circuit. The signals then enter a differential amplifier, a low pass filter ( $f_c = 7.2$  Hz), and finally an op-amp buffer. The overall gain in this portion of the circuit was

found to be 74.8. The DC output of the lock-in amplifier is proportional to the amplitude of the **LIA\_in** signal. To achieve zero output for zero input, the DC offset of the LIA can be adjusted by applying a DC voltage (from the D/A converter) to the **DCOFF** input.



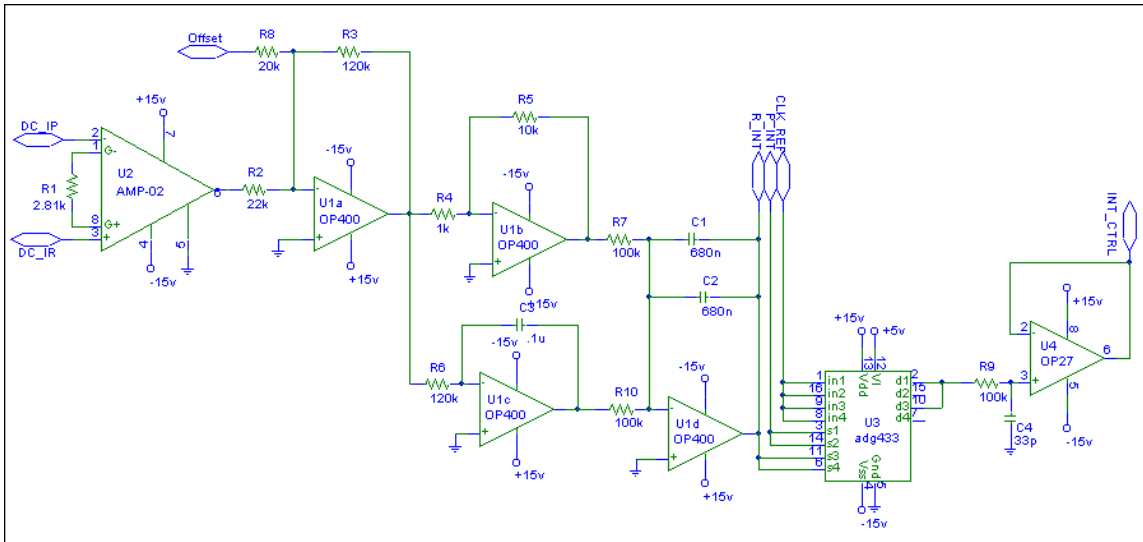
**Figure A.4: Operation of the Lock In Amplifier.** The gated and high pass filter version of **S\_SIG** is split into two branches. **CLK\_REF** is the switch control input for the **MAX4526** analog switch. The positive part of **S\_SIG** is selected for the **Y** output of the analog switch, and the negative part appears on the **X** output.



**Figure A.5: The Lock In Amplifier is a phase-sensitive detector and low pass filter that subtracts one phase of the transient-gated SLD signal from the other.**

### A.1.1.3 PIC Intensity Controller

The Proportional-Integral Intensity Controller is used to control the Reference Intensity (**R\_INT**). We wish to be able to set the difference between the signals **DCIP** and **DCIR**. Expressed differently, we want to control the difference in light intensity between the Principal and Reference wavelength phases before the light enters the sample. This is so that we can equilibrate the light intensity at the *exit* of the sample during the balancing stage of the measurement. The input to the PIC is the difference in intensity between the two phases as measured at the Input Light Detector. This circuit is shown in Figure A.6. This difference is obtained by putting the signals **DCIP** and **DCIR** into a differential amplifier (AMP-02, Analog Devices). This differential amplifier has a gain of approximately 14. (Gain =  $1+50k/2.81k$ ). This signal, **I\_AC**, is then put into a summing amplifier with **OFFSET**. Both signals have a gain of approximately 6 through the summing amplifier. The summing amplifier uses a section of an OP400 (Burr-Brown), which is a quad op-amp. The circuit then branches into a proportional branch with a gain of 10, and an integrator branch. The two branches are then added into a version of a summing amplifier. The summing amplifier has capacitors in the feedback to set a bias. This is necessary because we do not want a zero output on **R\_INT** for a zero input on the PIC. The capacitor in the output integrator charges to a value that is necessary to provide the proper Reference Intensity. The proportional, integral, and summing circuits use the other three op-amps in the OP-400 package. At this point, the output of the PIC is equal to the Reference Intensity control signal **R\_INT**. The overall effect is that the system sets the signal **R\_INT** so that **DCIR** is equal to **DCIP** minus  $1/10^{\text{th}}$  of the value of **OFFSET**. It is now time to mix **R\_INT** with the Principal Intensity control signal **P\_INT**. This is done with an analog multiplexer, the ADG433 (Analog Devices). This IC has two normally open (NO) contacts, and two normally closed (NC) contacts. The switches are all connected to the **CLK\_REF** signal. The NO switches are connected to **P\_INT**, while the NC switches are connected to **R\_INT**. The outputs of the ADG433 are hooked together, and the result is a signal that consists of **P\_INT** during the Principal wavelength phase and **R\_INT** during the Reference wavelength phase. This signal is then low pass filtered ( $f_c=48$  kHz), and put into a follower. The follower uses an OP-27. The RC load attached to pins 10 and 7 of the ADG433 is needed to balance the load, thereby reducing reflective waves on the signal lines. The voltage divider/diode circuit is needed to limit the output voltage to a range of 0 – 10 V.



**Figure A.6: The Proportional Integral Control Loop adjusts the Reference Intensity ( $R\_INT$ ) to be equal to the Principal Intensity ( $P\_INT$ ) minus the value of the *OFFSET* signal. The analog switch then multiplexes  $P\_INT$  and  $R\_INT$  at the system clock frequency to produce the overall intensity control signal ( $INT\_CTRL$ ) that is sent to the RF generator.**

#### A.1.1.4 Data Acquisition Circuitry

Software processing of the data is necessary to obtain the urea concentration measurements. We must therefore convert the analog signals into digital signals so that they can be sent to the PC for processing. Conversely, the PC must be able to control the hardware setup. Since a PC is not capable of generating an analog voltage, digital to analog converters are required as well.

In all, nine signals must be sent to the computer:

- The four DC intensity signals (**DCSP**, **DCSR**, **DCIP**, **DCIR**),
- The two temperature reading signals (**TEMP1**, **TEMP2**),
- The output of the PIC Intensity Control Loop (**R\_INT** or **LOOP**),
- The position control signal from the Space Age Controls® feedback device, **POSITION**,
- The Optical Bridge signal (**LIA\_OUT**, also known as **AC**).

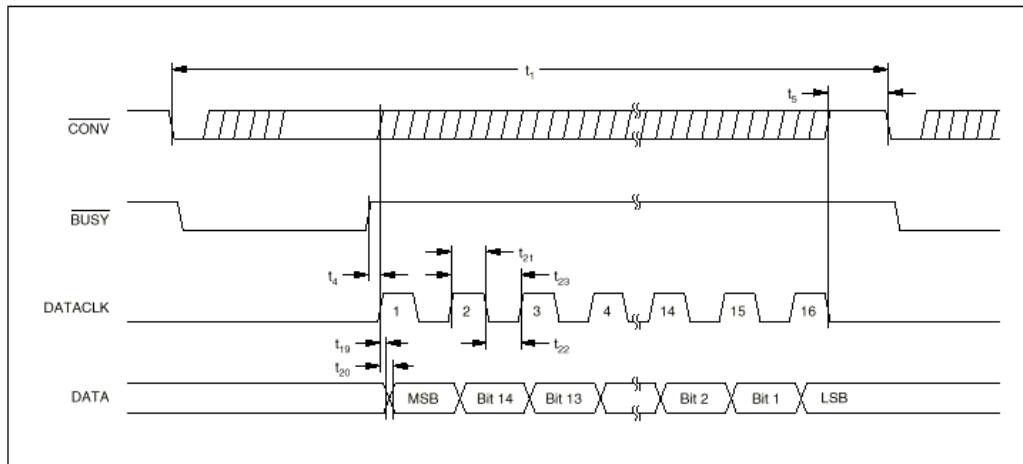
For all signals except **LIA\_OUT**, 1 mV of resolution is sufficient. These signals will be used mainly as normalization and correction factors by the urea concentration algorithm. (See Chapter 9.) For **LIA\_OUT**, 16-bit accuracy is required. Previous glucose studies done on NIV prototype instrument have indicated that 1 mV of signal translates to approximately 5 mg/dl of glucose. This indicates that the sensitivity is approximately 0.2 mV/mg/dl. Over a range of  $\pm 10V$ , a 16-bit converter would yield a theoretical accuracy of 1.5 mg/dl.<sup>†</sup> (The resolution of a 16-bit converter over 20 V is .305 mV.) The sensitivity

<sup>†</sup> Due to system noise, this accuracy has not yet been achieved with an *Optical Bridge* system. The system is limited by the optical detector noise, not quantization noise. Optical detector noise is mainly a function

to urea is expected to be similar to that of glucose. There are three signals that the PC must be able to control. The first is **P\_INT**, the Principal Intensity. This is the intensity of the light beam during the Principal wavelength phase. The second is **OFFSET**, the signal that sets the difference between **P\_INT** and **R\_INT**. The final signal, **DCOFF**, is used to control the system bias. (See § A.1.1.2.) A resolution of approximately 5 mV was chosen for **P\_INT** and **OFFSET**. This requires a 12-bit converter. While a finer accuracy is required for **DCOFF**, this is achieved with a resistive divider ( $\approx 50:1$ ), rather than a separate converter.

The overall data acquisition circuit therefore contains one 16 bit A/D converter, one 8 channel, 12 bit A/D converter, and one 4 channel 12 bit D/A converter. When selecting these devices, one factor became apparent quickly. All data transfer must be accomplished through the PC's parallel port. This means that only 18 data lines are available to generate chip select signals, select channels, receive/transmit data, etc. For this reason, we needed to use serial data converters. These devices send out and receive their data in a stream of bits, rather than on a sequence of pins.

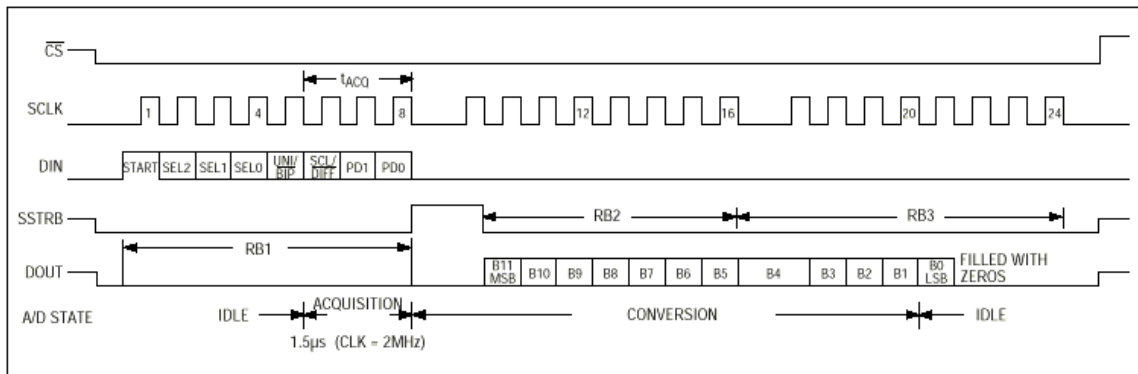
The device that was chosen as the 16-bit A/D converter was the AD7813 (Burr-Brown). This device has a selectable input range. As it is configured in Figure C.2.11, the input range is  $\pm 10V$ . This yields a resolution of 0.305 mV. In order to start a conversion, the input **CS\_AD16** is pulled low. This input is used both as a chip select and a conversion start signal. When the conversion is finished, the device pulls the **BUSY** pin low. The PC is monitoring the status of this pin, and once it is activated, the PC sends out a clocking signal (**SCLK**) in order to read the data. The AD7813 sends out one bit of the conversion for each low to high transition of **SCLK**. The data appears on the **AD\_DATA** line, which is then read back to the PC through the parallel port. Figure A.7, below, shows a typical conversion timing sequence for the AD7813.



*Figure A.7: Conversion timing sequence for the AD7813. (Figure taken from the AD7813 datasheet).*

of detector area, temperature, and bandwidth. Quantization noise depends only on the number of bits in the converter.

The MAX 186 (Maxim) was selected as the 8 channel 12 bit converter. The operation of this device is slightly more complex than the AD7813, mainly because of the need to select the desired channel. This converter is configured to have an input range of  $\pm 2.048V$ , for a resolution of 1 mV. In order to start a conversion, the chip is activated by pulling **CS\_AD12** low, and an 8 bit serial word is then written to the pin **DIN**. This serial word selects the conversion channel (0-7), the clock source (external or internal) and the conversion format (unipolar or bipolar, single ended or differential). The actual format of the control word is discussed in Appendix B. The conversion is finished when the converter pulses the **SSTRB** pin high for one clock cycle. The PC is monitoring the **AD\_STATUS** line. Once this line pulses high, the MAX186 will begin outputting the data, one bit per pulse of the **SCLK** line. The data has one leading zero and three trailing zeroes that frame the conversion result. The data is read back to the PC using the **AD\_DATA** line. Figure A.8 shows the conversion timing for a MAX186 conversion sequence.



**Figure A.8:** A typical conversion timing sequence for the MAX186. (Figure taken from the MAX186 datasheet)

The final data conversion device is the 4 channel DAC. A DAC8420 (Analog Devices) was chosen for this purpose. This device requires a  $\pm 10V$  reference (the AD688, also from Analog Devices). In order to update the DAC voltage, **CS\_DA** is pulled low. A serial word is then sent to the device. This is a sixteen bit word. The first two bits select the channel, the next two are don't care bits, and the final twelve bits set the voltage. The bits are clocked in on the **SDATA** line at each transition of **SCLK**. Finally, the **LD\_DA** signal is pulled low, which initiates the converter update. The range of this converter is  $\pm 10V$ , yielding a resolution of  $\approx 5$  mV. A typical conversion timing sequence for the DAC8420 is shown in Figure A.10. The full data acquisition circuit is shown in Figure A.9.

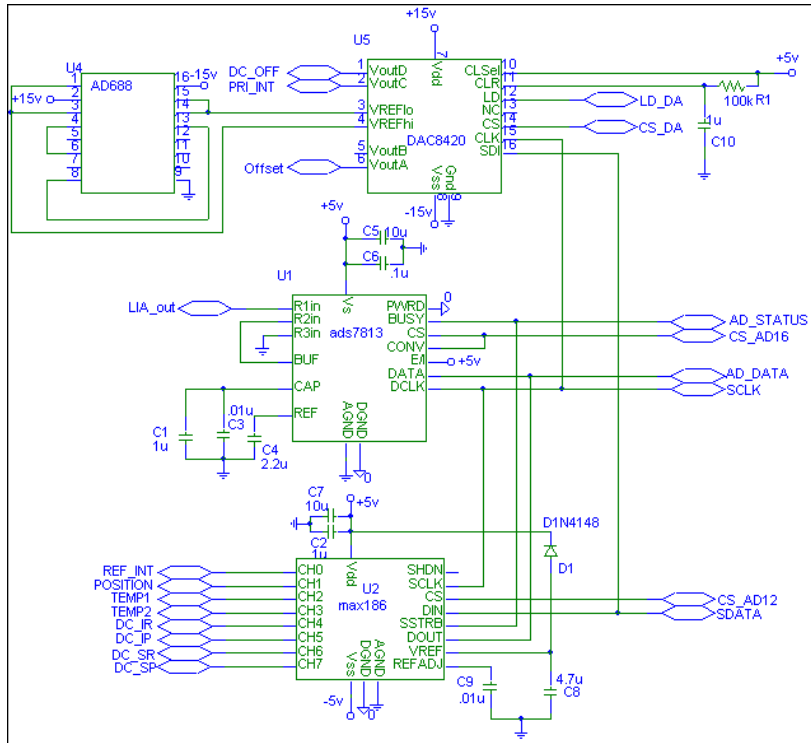


Figure A.9: The data acquisition circuitry consists of one 16 bit A/D converter, one 8 channel, 12 bit A/D converter, and one 4 channel, 12 bit D/A converter.

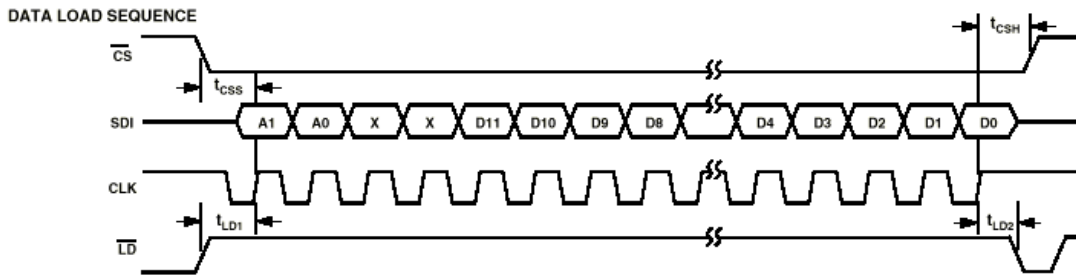
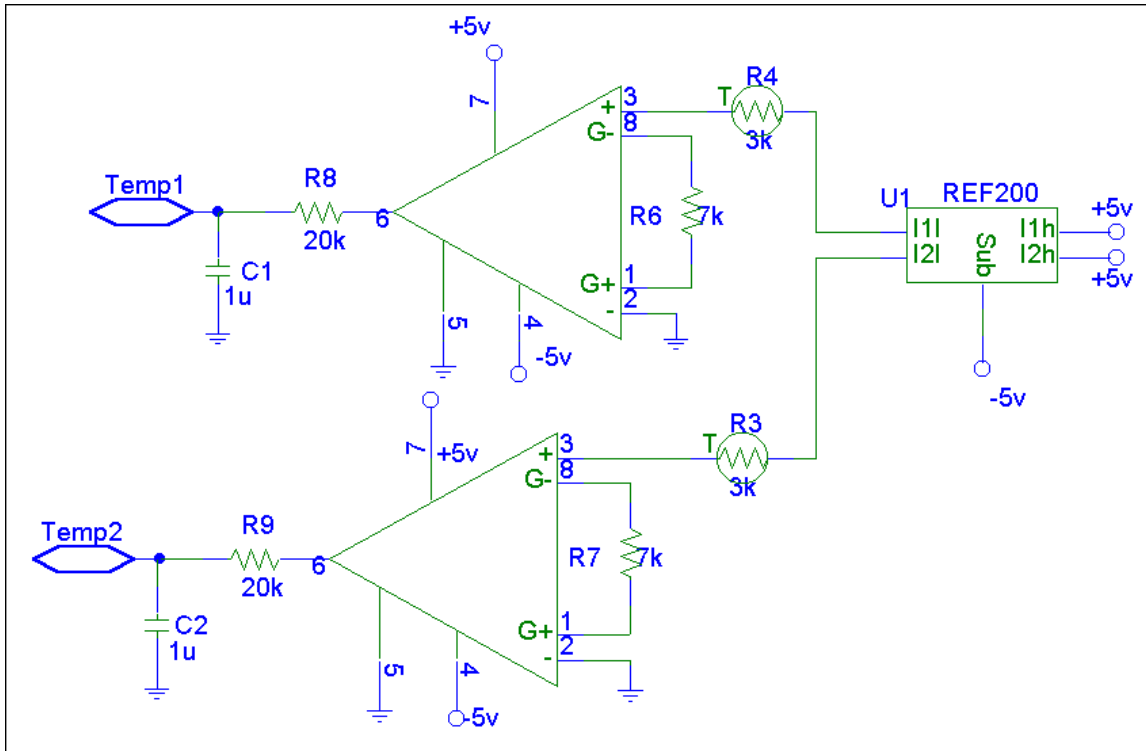


Figure A.10: Conversion timing sequence for the DAC8420. (Figure taken from the DAC8420 datasheet).

#### A.1.1.5 Temperature Monitor

Since the measurement is sensitive to temperature variations, it is necessary to monitor and control the system temperature. Two  $3\text{k}\Omega$  thermistors are used, one in the spent dialysis fluid, and the other in the clean dialysis fluid. Thermistors generally have a negative temperature coefficient, which means that as the temperature surrounding the thermistor increases, the resistance decreases. The thermistors are supplied with a constant  $100\ \mu\text{A}$  current, which is obtained from a REF200 (Burr-Brown). The REF200 has two  $100\ \mu\text{A}$  constant current sources. The voltage on the thermistor is put into an AMP-02 instrumentation amplifier (PMI). The maximum voltage that will appear on the thermistor is  $0.3\text{V}$  ( $100\ \mu\text{A} \cdot 3\ \text{k}\Omega$ ). The A/D converter can handle a maximum of  $2.048$

V, so a signal amplification of approximately 8 can be safely used. The gain equation for the AMP-02 is  $G = 1 + 50k/R_g$ .  $R_g$  was selected to be  $7k\Omega$ . The output of the instrumentation amplifier is also low pass filtered ( $f_c = 8 \text{ Hz}$ ).



**Figure A.11: The temperature monitoring circuitry consists of a constant current source, thermistor, and instrumentation amplifier.**

#### A.1.1.6 Connectors to the Analog Board

The analog board has two connectors that receive and transmit signals to other electronics in the system. There is a 25 pin DB-25 connector that connects to the digital board, and a 14 pin lock type connector that receives signals from the two optical detectors and the thermistors. There is also a 5 V/ground power connector. Note: The  $\pm 15V$  power that is required for many of the analog circuits is generated by a special module on the analog board. This module, the SP7015 (Analogic) accepts a 5V input, and produces the necessary 5V and  $\pm 15V$  power. The signal connections to the digital board are given in Table A.1. The signal connections to the optical detector are given in Table A.2. The name, connector pin, and function of each signal are given in the tables.

**Table A.1: 25 Pin Digital Board Connector Signal List**

<b>Signal Name</b>	<b>Pin</b>	<b>Function</b>
CLK_P	1	Clock signal for identifying the Principal Phase
CLK_R	2	Clock signal for identifying the Reference Phase
NC	3	No Connect
CLK_REF	4	4 kHz System Clock
NC	5	No Connect
NC	6	No Connect
AD_DATA	7	Transmits bit stream from the A/D converters
CS_AD12	8	Chip Select signal for the MAX186
CLK_G	9	Transient gating clock signal
SDATA	10	Serial Data
SCLK	11	Serial Clock
INT_CTRL	12	Light Intensity Control Signal
Vs+	13	+15 V supply voltage
NC	14	No Connect
NC	15	No Connect
LD_DA	16	Causes D/A converter to update its value
NC	17	No Connect
NC	18	No Connect
NC	19	No Connect
AD_STATUS	20	Indicates whether an A/D conversion has completed
CS_DA	21	Chip Select signal for the DAC8420
CS_AD16	22	Chip Select signal for the ADS7813
NC	23	No Connect
AGND	24	Analog Ground Signal
Vs-	25	-15 V supply voltage

**Table A.2: 14 Pin Signal Connector Pin List**

<b>Signal Name</b>	<b>Pin</b>	<b>Function</b>
NC	1	No Connect
POSITION	2	Space Age Controls Position Feedback
NC	3	No Connect
NC	4	No Connect
TEMP_RET	5	Thermistor ground return signal
TEMP1	6	Thermistor 1 signal
GND	7	Ground
TEMP2	8	Thermistor 2 signal
I_SIG_RET	9	Input Light Detector ground return signal
I_SIG	10	Input Light Detector signal
S_SIG_RET	11	Sample Light Detector ground return signal
S_SIG	12	Sample Light Detector signal

Vs-	13	-15V power signal
Vs+	14	+15V power signal

### A.1.2 Digital Board

The Digital Board is responsible for optically isolating the instrument from the PC, generating communication between the instrument and the PC, and generating control signals for the analog board. It is a two layer Printed Circuit Board. The dimensions of the board are approximately 4" by 6". This section describes the sub-modules that make up the digital board.

#### A.1.2.1 Optical Isolation and Parallel Port Interface Unit

The hardware of any medical device that includes connections to a PC must be optically isolated from the PC. This is for two reasons: First, it is necessary to protect the patient from any current spikes and/or leakage currents that may cause a shock hazard. Second, noise from the PC would infect the rest of the electronics. For this reason, all lines that connect the PC to the hardware have been optically isolated using the HCPL2231 (Hewlett-Packard). This is a dual digital optical isolator. The optical isolation unit consists of a low pass filter ( $\tau = 1\mu\text{s}$  or  $f_c = 318\text{ kHz}$ ), buffer (usually a 4010 or an 'ALS16), and the optical isolator. The common 5V supply (its ground is connected to the chassis ground) is generated by another Burr-Brown IC, the DCP0105.

The parallel port (LPT) connection is used to transmit all data between the PC and the rest of the instrument. The connector pinout is given below in Table A.3. A second method of interface is also available. This connection is to a microcontroller, but this option is not used at this time.

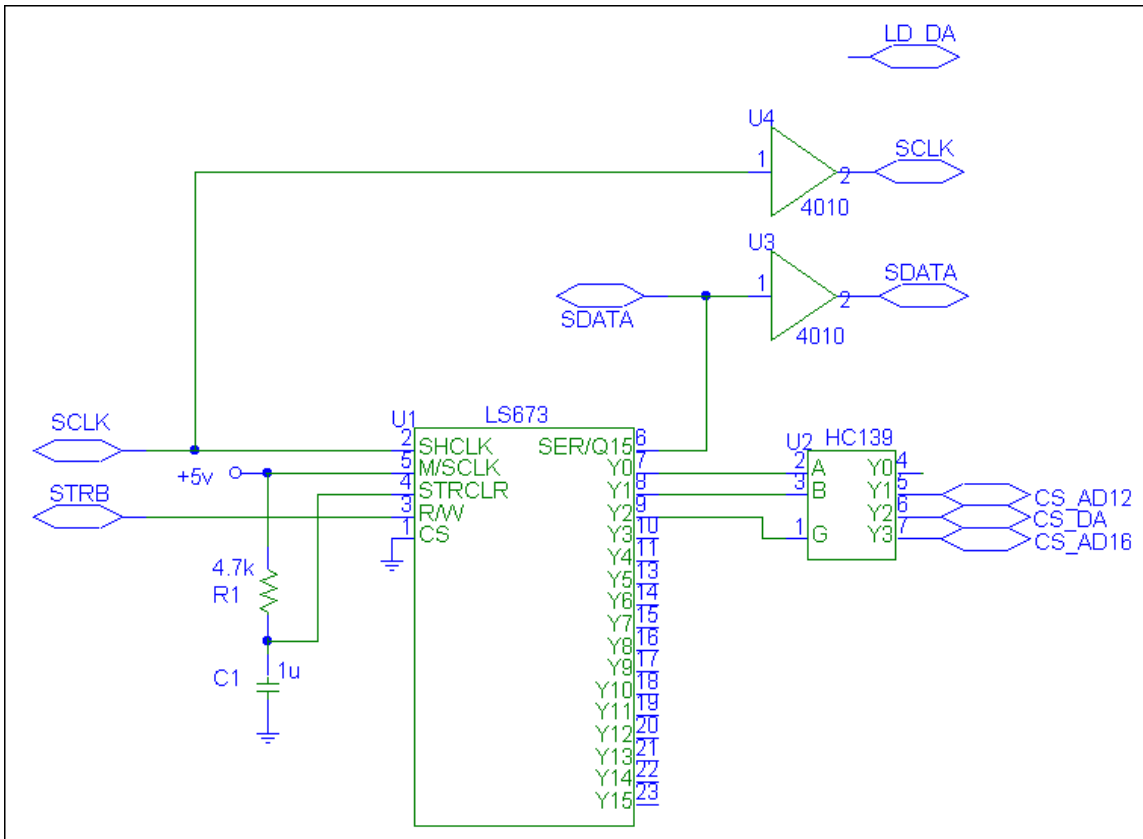
**Table A.3: Parallel Port Connector Pin List**

Pin	Signal Name	Function
1	NC	No Connect
2	STRB	Chip Select Update Signal
3	LD_DA	D/A converter update signal
4	SCLK	Serial Clock
5	SDATA	Serial Data
6	NC	No Connect
7	PUMP_A	Pump Control Signal A
8	PUMP_B	Pump Control Signal B
9	MOT_EN	Motor Enable
10	NC	No Connect
11	LIMIT	Motor Limit Switch
12	AD_DATA	Data Signal from the A/D converters
13	AD_STATUS	Conversion finished signal
14	NC	No Connect
15	NC	No Connect
16	PP_EN	Enables the parallel port interface
17	UC_COM	Enables control by a microcontroller

18	NC	No Connect
19	GND	Signal Ground
20	GND	Signal Ground
21	GND	Signal Ground
22	GND	Signal Ground
23	GND	Signal Ground
24	GND	Signal Ground
25	GND	Signal Ground

#### *A.1.2.2 Device Select Circuitry*

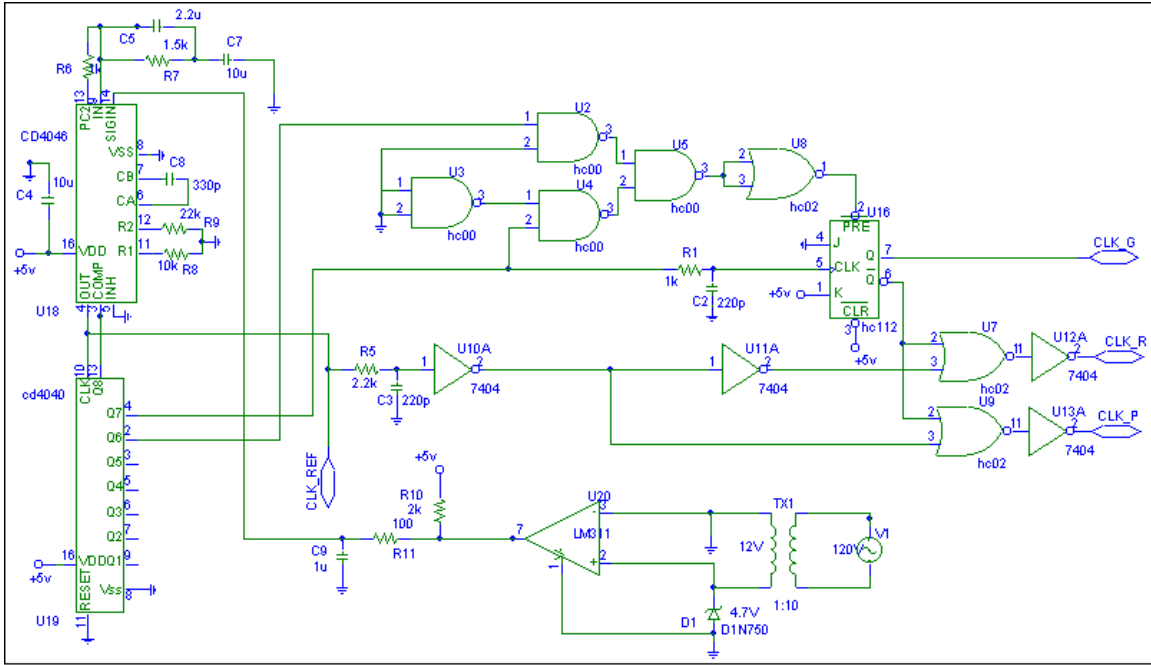
In order to generate the chip select signals that are needed by various devices on the analog board, a decoding system is needed. Since we do not have extra pins in the parallel port interface, we send a serial code word, which is then converted to a chip select signal. Figure A.12 shows the decoder circuit. The data is input to a serial to parallel converter chip on the **SDATA** line, and is clocked into the chip using the **SCLK** line. When the correct number of bits has been sent, the **STRB** signal is activated to latch the output onto the LS673. A second level decoder is used to select the proper chip select signal. The signals **LD\_DA**, **SCLK**, and **SDATA** are also sent to the analog board for device selection. While the circuit in Figure A.12 may appear to be overkill, some unused signals have been omitted for clarity. The extra lines also allow room for expanded functions of the device.



*Figure A.12: This decoder is used to generate chip select signals for the data acquisition circuitry. The signals SCLK, SDATA, and LD\_DA are also used to control the data acquisition circuit.*

### A.1.2.3 Clock Generator

The clocking signals **CLK\_REF**, **CLK\_P**, **CLR\_R**, and **CLK\_G** have been previously discussed. The circuit in Figure A.13 shows how these signals are generated. This circuit was originally designed to operate around 1 kHz. However, during hardware testing, it was discovered that the system suffered from significant 60 Hz noise contamination. It was therefore decided to synchronize the system clock to the 60 Hz line voltage signal. The circuit in Figure A.13 converts the 120V, 60 Hz line voltage into a 5 V square wave. The signals **CLK\_REF**, **CLK\_G**, **CLK\_L** and **CLK\_H** are then generated by the circuit. A phase locked loop (CD4046) in conjunction with a ripple counter (CD4040) is used to generate 120 Hz and 240 Hz signals from the original 60 Hz. (In order to generate a 25% duty cycle signal such as **CLK\_L**, a 240 Hz signal is required.



*Figure A.13: The clock generator circuit generates a 60 Hz square wave (CLK\_REF), in addition to the demultiplexing signals CLK\_P and CLK\_R. It also generates the transient gating signal CLK\_G.*

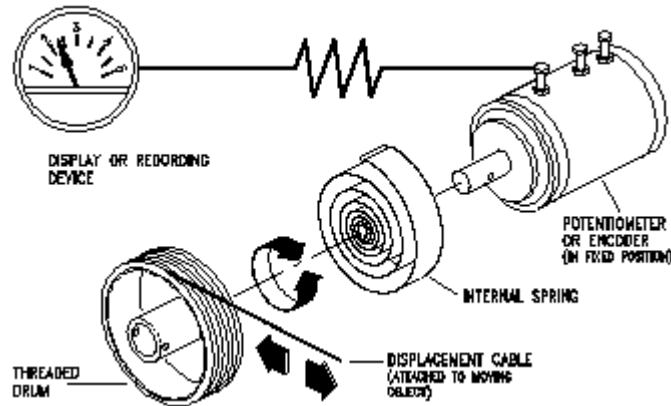
*A.1.3 Motor and Pump Controller*

In order to make changes to the optical pathlength, a position control system is required. The movement of fluid in the system also requires a special fluid transfer system. This dissertation includes a description of the physical and mechanical design of this system, including the position and fluid control systems. The position control system uses a unipolar, 200 steps/revolution stepping motor. A separate controller board provides the interface to this motor. The controller board, which is approximately 1.25” square, contains one IC and three signal connectors. A separate device provides position feedback to the computer. This device will be described later in this section

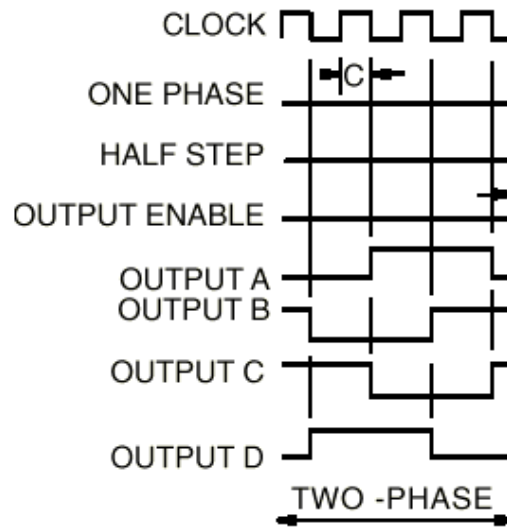
The first connector is for the motor windings. A unipolar stepper motor has four windings. The windings are connected in pairs, and a center tap wire is also present. By energizing these windings in the proper sequence, the motor shaft will turn. In order to simplify the motor drive, a specialized IC, the UCN5804 (Allegro Microsystems) was used. The ‘5804 is a stepper motor translator/driver. It has two mode select lines, an output enable pin, a direction control input, and a step input. When the output is enabled, a pulse on the step input line causes the chip to send out a sequence of pulses on the four outputs that energize the windings in the proper order. See Figure A.15 for a timing diagram. The second connector on the motor control board has five pins. The first is **MOT\_CLK**, which is the step input signal. It is generated by the digital board by combining two other signals: **SCLK** and **MOT\_EN**. The second motor control signal is **DIR**, which selects the direction that the shaft will turn. This signal is generated by combining the **MOT\_EN** signal and the **SDATA** signal. The third and fifth pins are

ground and power connections, and the fourth pin is a **LIMIT** signal, which indicates when the motor has reached its movement limit. The final connector is a power connector for the motor (+12 VDC). Figure A.16 shows the schematic diagram of the motor control circuit.

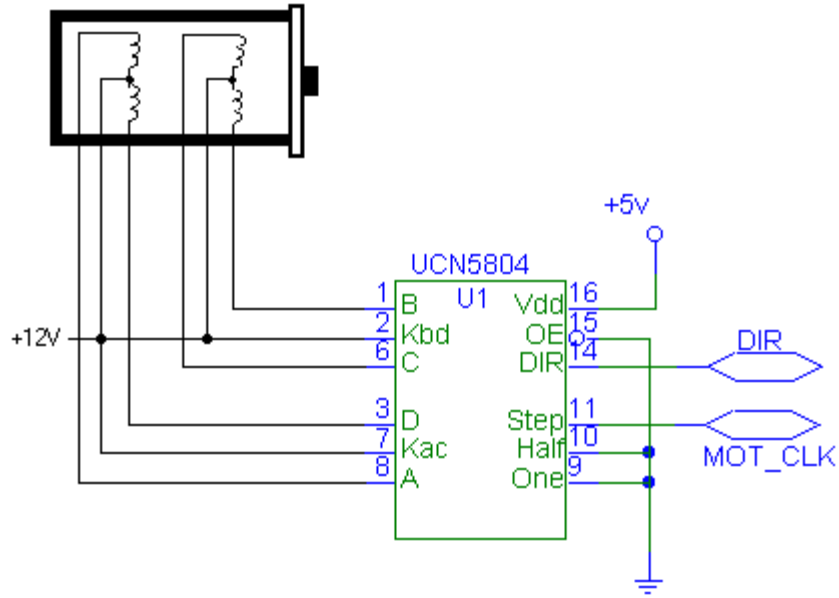
In order to obtain precise position information, a feedback device was required. The Space Age Controls position transducer model # 150 was selected for this purpose. This device consists of a linear potentiometer (full scale value: 5 k $\Omega$ ) that is connected to a cable that is wound on a rotating drum. As the fixed end of the cable is unwound from the drum, the resistance of the potentiometer changes. This is illustrated in Figure A.14. The potentiometer is connected to a simple voltage divider circuit, and amplified to cover a -2V to +2V range. It is then sent directly to the MAX186 analog to digital converter.



*Figure A.14: Schematic diagram of the Space Age Controls (R) model 150 rotating drum potentiometer.*



*Figure A.15: Timing diagram showing the sequence of energizing windings carried out by the UCN5804. (Taken from the UCN5804 datasheet).*



*Figure A.16: Circuit Diagram for the Stepper Motor Driver.*

The fluid control circuit also uses a stepper motor, but this is a bipolar motor. A bipolar stepper motor requires a drive voltage that switches between positive and negative values on successive steps. A different type of driver is required to move the pump motor in this case. In order to advance the pump motor one click, a sequence of four signal transitions is required. The full step wave drive mode is used, which provides maximum torque as both motor windings are energized at all times. The step transition sequence is: AB, AB\*, A\*B\* AB\*, where A and B represent logic high on **PUMPA** and **PUMPB** respectively, and A\* and B\* represent logic low. **PUMPA** and **PUMPB** are generated by an Altera™ chip located on the pump controller board. See Appendix C for the VHDL code and device pinout. The Altera™ chip also controls the operation of four pinch type solenoid valves which control the filling and emptying of the measurement cuvette. **PUMPA** and **PUMPB** are then fed to a circuit designed around National Semiconductors LMD18245 H-Bridge Motor Driver. Two of these interface chips are required to drive the circuit, one for each winding of the motor. The circuit is shown in Figure A.17.

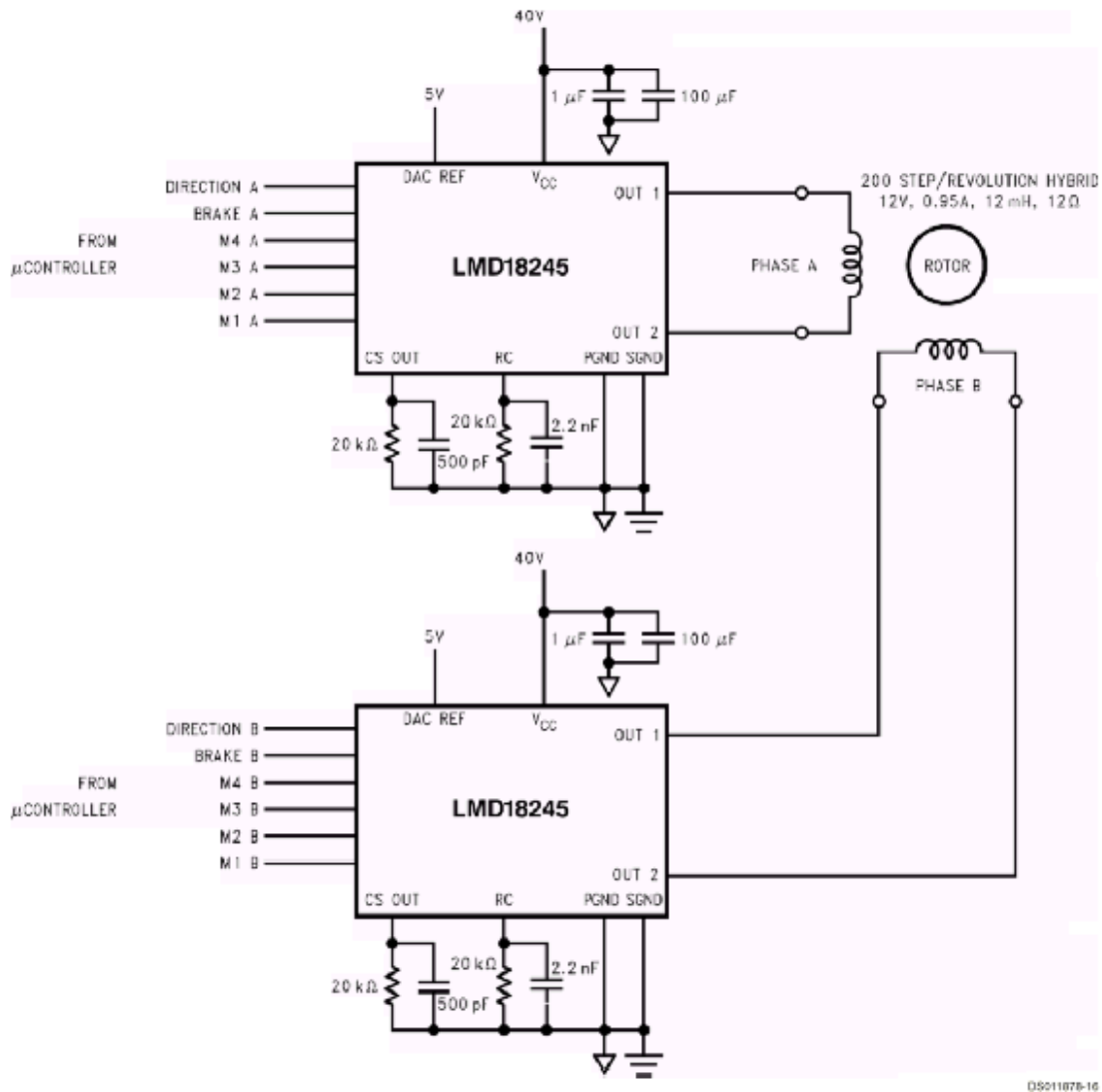


Figure A.17: The pump controller driver circuit, taken from the LMD18245 data sheet.

#### A.1.4 RF Signal Generator

In order to control the intensity and wavelength of the light that reaches the sample, the AOTF requires a Radio Frequency (RF) signal. This signal needs to be fairly high powered ( $\sim 3W$ ), and have a frequency in the range of 50-150 MHz. A commercial RF driver from NEOS Technologies was used for this purpose. This device accepts a 0-1 V analog input for the intensity control, and a 32 bit digital word for the frequency control. The intensity control input is the **INT\_CTRL** signal that has been previously discussed. It is also digitally isolated using an ISO122 analog optical isolator and buffered with an LT1010 (Linear Technologies) buffer amplifier. The frequency control is done through a separate card that resides inside the PC on the ISA bus with a base address of 0x400. It has an external input that is connected to **CLK\_REF** that indicates which wavelength (Principal or Reference) is being activated. It sends a 32-bit frequency control word for each part of the **CLK\_REF** cycle. It also receives updates from the PC to the frequency word. This frequency word has been mapped in the software to the desired wavelength.

The NEOS driver is capable of generating frequencies from 20-200 MHz. The NEOS driver receives the 32-bit word, converts it to a frequency, and gives the output signal the desired amplitude. The NEOS driver is only capable of producing 1.5W however, so an external RF power amplifier is required. The ZHL-03-5WF RF power amplifier from MiniCircuits, Inc., (Brooklyn, NY) is used to boost the signal output to the required 3W. This signal is then sent to the AOTF.