

Radio Design and Performance Analysis of Multi Carrier-Ultrawideband (MC-UWB) Positioning System

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BIOGRAPHY

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Dr. William R. Michalson is an Associate Professor in the ECE Department at the Worcester Polytechnic Institute where he performs research and teaches in the areas of navigation, communications and computer system design. He supervises the WPI Center for Advanced Integrated Radio Navigation (CAIRN) and is the Director of the WPI Bioengineering Institute's Center for Untethered Healthcare. His research focuses on the development, test, and evaluation of systems, which combine communications and navigation. He has been involved with navigation projects for both civilian and military applications with a special emphasis on navigation and communication techniques in indoor, underground or

otherwise GPS-deprived situations. Prior to joining the faculty at WPI, Dr. Michalson spent approximately 12 years at the Raytheon Company where he was involved with the development of embedded computers for guidance, communications and data processing systems for both space borne and terrestrial applications.

ABSTRACT

This paper continues discussing the design and development of an advanced integrated wireless system discussed in papers [1, 2, 3] that can be used by emergency responders and health care providers to communicate useful and critical information whenever and wherever they need. The design of a Multi Carrier signal structure and signal processing algorithm that applies a matrix-decomposition-based Multi Carrier range recovery algorithm to obtain a super resolution location solution is discussed in [1], system performance aspects of the Multi Carrier – Ultrawideband (MC-UWB) approach to precise positioning are presented in [2]. The design and performance evaluation of the proposed RF front end receiver structure being developed for precision location system using this Multi Carrier technique is discussed in [3].

This paper presents the recent developments and current progress of the precise position location system, focuses on improvements in the previously presented RF front end structure [3] and describes the design of the required digital back end of the receiver structure. The design and performance of the entire receiver structure and a high level overview of the transmitter structure are presented in this paper. The designed prototype system is very well suited for real time position location and tracking of first responders and emergency rescuers, within one meter accuracy.

problems with a single carrier signal structure is that as the symbol rate increases the symbol interval becomes shorter than the delay spread. A Multi Carrier signal structure solves this problem by decreasing the symbol rate and increasing the number of carriers. The basic idea behind the OFDM signal is to take a signal and send it over multiple low rate carriers instead of a single high rate carrier. An OFDM signal consists of many sinusoidal subcarriers. These subcarriers are orthogonal and therefore do not overlap with each other. The advantages of using a Multi Carrier signal structure are listed below:

- Improved spectral efficiency
- Robust in fading environment
- Simplified equalization needed
- High data rate can be achieved
- Signal generation is simple

The structure of the OFDM signal proposed is of the form:

$$s_c(t) = \sum_{m=0}^{M-1} A_c e^{2\pi j(f_c + m\Delta f)t + \phi_m} \quad (1)$$

where M is the number of sinusoidal carriers with frequency spacing Δf and each carrier has arbitrary phase ϕ_m . The signal proposed occupies a very wide bandwidth but each subcarrier occupies a very low portion of the total band and hence the name Multi Carrier – Ultrawideband (MC-UWB). If the OFDM signal has M subcarriers then the true bandwidth of the signal is equal to $(M*60 \text{ kHz})$, assuming that the 99% power bandwidth of each sinusoidal tone is approximately 60 kHz. The unoccupied frequency spectrum of Δf between two subcarriers can be used by other services; likewise the OFDM subcarriers can be carefully placed in the frequency spectrum which is already being used, such that it does not interfere with existing services.

The OFDM baseband signal is generated at the transmitter and is received by a direct downconversion receiver. The transmitter uses an IDFT to generate N time samples which are repeatedly transmitted to form the continuous output waveform. Figure 2 shows three subcarriers of the generated OFDM frequency spectrum where the frequency spacing Δf of the successive non overlapping OFDM subcarriers is set to 244 kHz, which is approximately equal to about 20 Narrowband FM channels.

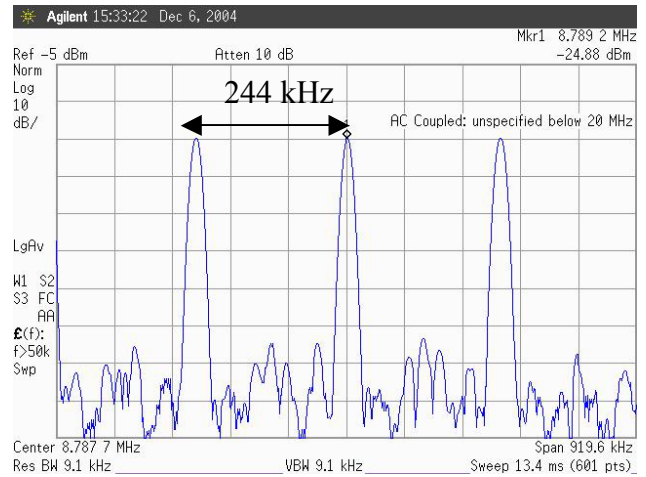


Figure 2: Subcarriers of Generated OFDM signal

The unoccupied spectrum in between any two subcarriers can be utilized by other services. The characteristics of the generated MC-UWB signal currently being used are listed in Table 1.

Table 1: MC-UWB Signal Characteristics

Number of Subcarriers	50 Sinusoids
Subcarrier Spacing	244 kHz
First Subcarrier at	2.44 MHz
Last Subcarrier at	14.64 MHz
Occupied Signal BW	12.2 MHz
OFDM signal period	40.96 usec

For initial testing the OFDM signal generated consists of 50 sinusoidal subcarriers, where the subcarriers are spread over 12.2MHz but the actual spectrum occupied is only 3MHz (50 * 60 kHz). The frequency spacing Δf and the number of sinusoidal carriers M can be varied very easily in software resulting in a very simple implementation of MC-UWB signal whose bandwidth can be varied easily.

The proposed precise positioning system uses this MC-UWB signal discussed above. The system uses four or more receivers to calculate a three dimensional position of the transmitter, worn by each first responder, the challenge being able to locate the position of the first responder to a resolution of one meter or less. The position location algorithms are based on Time Difference of Arrival technique (TDOA). The system performance aspects of the MC-UWB approach are discussed in [3]. Discrete Fourier Transform (DFT) processing is used at the receiver to demodulate the transmitted OFDM signal. The OFDM based receiver structure is shown in Figure 3. The received signal is downconverted, sampled and loaded in a PC where FFT processing and TOA estimation is implemented.

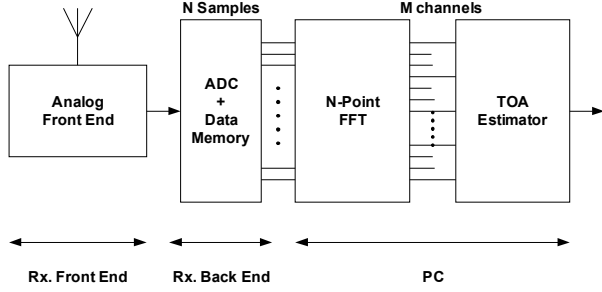


Figure 3: OFDM Based Receiver Structure

We consider the case of real signals only and therefore describe the signal structure as shown:

$$s(t) = s_c(t) + s_c^*(t) \quad (1)$$

$$s(t) = \sum_{m=0}^{M-1} A \cos(2\pi(f_o + m\Delta f)t + \phi_m) \quad (2)$$

where $s_c(t)$ is the signal as defined in equation (1) and $s_c^*(t)$ is its conjugate. This transmitted signal is received at four or more receivers located at various sites, with distances d_k from the transmitter giving rise to propagation delays $\tau_k = d_k / c$. These delays result in phase shifts in each subcarrier component of the MC-UWB signal received at different receiver sites. As discussed and derived in detail in [2], this phase shift depends upon τ_k and the subcarrier frequency. The difference of phases obtained for a subcarrier at two different receiver sites is $\theta_{12} = \Delta\theta_1 - \Delta\theta_2$ from which TDOA estimates are calculated at those sites,

$$\Delta\tau_{12} = \frac{-\theta_{12}}{2\pi\Delta f} = \frac{d_2 - d_1}{c}$$

where, c is the wave velocity. The problem of TDOA estimation thus reduces to estimation of consistent phase change between the adjacent subcarriers in the received signal, which is implemented using direct state space estimation approach [1, 2]. Given the signal structure and the concept behind the signal processing algorithms, the current work focuses on the MC-UWB receiver and transmitter's front end and the back end design and development that are discussed in next sections.

RECEIVER FRONT END DESIGN AND DEVELOPMENT

This section will focus on prototype design and development of the RF front end of the receiver suitable for MC-UWB precise positioning system. The initial analysis, design and implementation of wideband MC-UWB RF receiver structure was discussed in [3]. The

receiver front end consists of Band Pass Filter, Low Noise Amplifier, Automatic Gain Control, Downconverting Mixer and Low Pass Filter as shown in Figure 4.

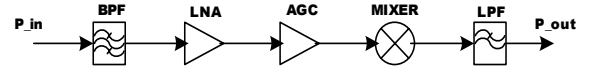


Figure 4: Receiver's RF Front End

The portable receiver antenna used is a unity gain antenna with a wide bandwidth from 400 MHz to 512 MHz. The RF bandpass filter (BPF) used is a triple tuned helical bandpass filter. The low noise amplifier (LNA) follows the BPF. The selection of the LNA is very crucial as the noise figure of the LNA sets the noise figure of the receiver. The LNA chosen has a high gain of 22.5 dB and a low noise figure of 1.6 dB (max). The wideband variable gain amplifier (VGA) that follows the LNA has a gain variation range from -11dB to 34dB and can be digitally controlled through a serial 8 bit gain control word. A high performance active mixer is used as a direct down-converter. The required local oscillator signal to drive the mixers should be between -12 dBm and -3 dBm. An RF PLL frequency synthesizer provides the mixer with the required local oscillator signal. The crystal oscillator used in the PLL synthesizer is a 10 MHz TCXO and has a frequency stability of 2.5 ppm. The VCO used in the PLL circuit has a frequency range of 415 MHz to 475 MHz, a tuning sensitivity of 10 MHz/V and the output phase noise is 136 dBc/Hz. The 2nd and 3rd harmonic suppressions at the VCO output are -18 dBm and -20 dBm respectively.

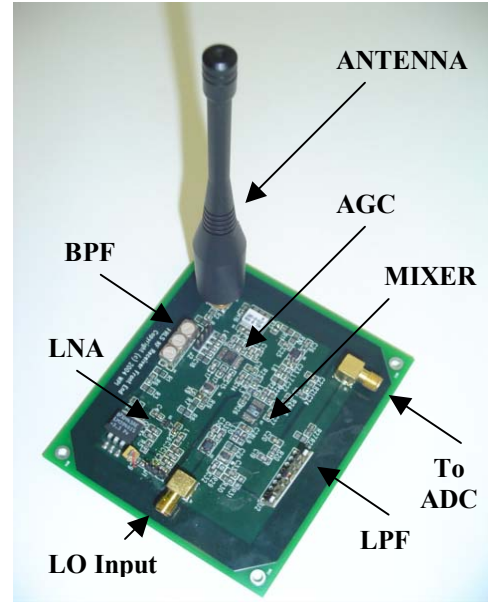


Figure 5: Designed RF Front End PCB

A 7th order LC lowpass filter follows the mixer. This LC filter is designed with a very sharp cut off and a very low insertion loss of 0.3 dB (max). The designed PCB for the receiver RF front end is shown in Figure 5 and was successfully tested.

The achieved receiver system parameters are as shown in Table 2. The output of the LPF is the input to the ADC which is discussed in the next section.

Table 2: RF Front End System Parameters

System Parameter	Achieved
System G (dB)	45
System NF (dB)	2.73
System IIP3 (dBm)	-20
Rx. Sensitivity (dBm)	-90
Rx. SFDR (dB)	47

The use of a “software radio” design approach makes the system less complicated and depending upon the wireless channel and the environment, it is possible to vary the signal bandwidth without any changes in the transmitter and receiver hardware. The effects of RF front end system parameters on location accuracy are discussed in [3]. The smaller signal bandwidths result in better receiver sensitivity and higher dynamic range, however these improvements come at the cost of deteriorating location estimate accuracy. Thus, an important tradeoff between the receiver sensitivity, dynamic range and the transmit power must be made to achieve the location accuracy goal of one meter. Figure 6 shows the effect of signal bandwidth on receiver sensitivity and the spurious free dynamic range.

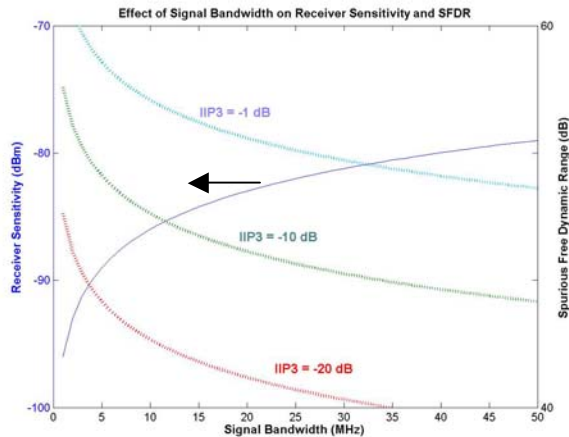


Figure 6: Effect of varying the Signal BW on Sensitivity and SFDR

RECEIVER BACK END DESIGN AND DEVELOPMENT

The receiver back end consists of a high-speed ADC board and a digital controller responsible for capturing and storing the ADC samples for transfer to a PC for analysis. We originally used the Maxim MAX108 ADC converter but after encountering problems we switched to the recently released National Semiconductor ADC081000 8-bit 1GSPS converter. This device uses less power and requires a single 1.9V supply instead of the multiple supplies required by the Maxim part. The converter also has a 1:2 demultiplexer that provides two 8-bit samples over a 16-bit LVDS bus at half the sampling rate. This allows the receiver in the FPGA to run at half the sampling rate, making for simpler timing constraints while also taking advantage of the inherent parallelism available in an FPGA.

The ADC081000 is packaged in a 128-pin exposed pad LQFP and we designed a custom 4-layer PCB for this ADC. The ADC connects to the digital controller board through a 40-pin header that is used for the 32 LVDS signals.

For the digital controller board we used a Xilinx Virtex II FPGA to implement most of the functions required for the data capture and storage of the ADC samples. We designed a custom 8-layer PCB for this board and added a 64MByte SDRAM, a 10/100 Mb Ethernet Interface, and an RS232 interface, as well as the usual power supplies and configuration PROM required by FPGA designs. When combined with the RF front end, a three PCB stack forms the complete MC-UWB receiver.

The FPGA we selected is a Virtex-II XC2V1000 device that has the equivalent of one million system gates. This capacity provides an excellent development platform for implementing our controller. Adding new features or making modifications just require downloading new bit stream through the JTAG interface. We are currently running the FPGA and SDRAM at 100MHz, although the board was designed to run at up to 250MHz providing for 500MBPS. All functions of the FPGA were designed using VHDL, synthesized and implemented using Xilinx ISE tools, and simulated using Modelsim.

Figure 7 shows a block diagram of the digital back end of the receiver.

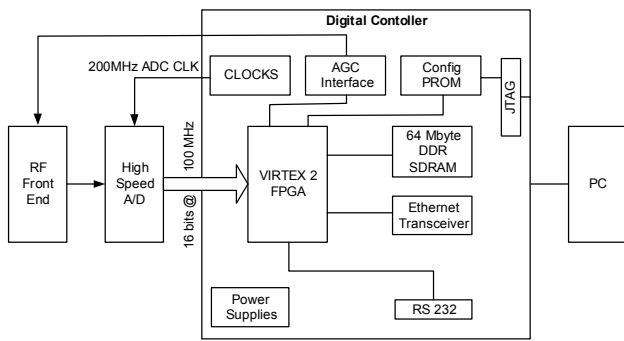


Figure 7: Detailed Receiver Back End Block Diagram

Figure 8 shows the PCB designed for the digital controller and identified the main components.

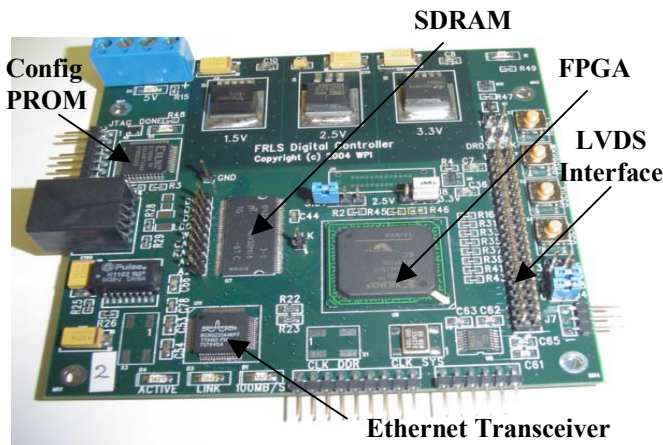


Figure 8: Designed Digital Controller PCB

The digital controller has to accept incoming data from the ADC converter at 100MSPS and is stored in the DDR SDRAM prior to being transferred to a PC for analysis. The data can not be simply streamed from the ADC converter into the SDRAM but instead is transferred into a dual port asynchronous FIFO, also implemented in the FPGA. A dual-port asynchronous FIFO is implemented in the FPGA. This FIFO serves two purposes: it converts the data samples from the converter clock domain to the SDRAM clock domain, and it provides temporary storage while the SDRAM is carrying out precharge or refresh operations.

After a number of OFDM symbols have been captured and stored in the SDRAM they need to be transferred to a PC for integration with other receiver samples to compute the TDOA estimates. Although the sample data will eventually be transmitted wirelessly over 802.11 we are currently using a simple RS232 interface to connect to a local PC. The data is read out of the SDRAM a row at a time. Each row corresponds to 1024 bytes and is stored in

another dual port FIFO before being transmit from the UART at 115kbaud.

The FPGA is also used to provide a number of other functions as shown in Figure 9. One of these is an automatic gain controller for the VGA in the front end. As discussed in the previous section the VGA can be operated in two modes, Low Gain Mode (-11dB to 17dB) and High Gain Mode (6dB to 34dB) with overlap between the two gain modes allowing some flexibility in choosing the operating mode. The dynamic range of the data converter in the back end is affected by the percentage of the full scale range (%FSR) utilized by the signals at the input to the data converter. The %FSR is dependant upon the gain provided by the receiver front end. Thus an AGC implementation of the digitally controlled variable gain amplifier in the RF front end is required for maximizing the FSR utilization. Its primary objective is to balance the amplification or the attenuation of the received OFDM signal such that it utilizes the maximum range for the ADC converter chosen for the receiver RF front end. The digitally controlled VGA requires an SPI interface which transmits an 8 bit gain code. The 8 bit gain code is calculated from the previous OFDM signals which were converted into digital samples.

Originally a complex state machine was implemented to provide overall control of all the data capture and transfer operations in the FPGA. As this becomes increasingly complicated as we added more features and requirements, we have replaced the state machine with a Picoblaze 8-bit microcontroller (also described in VHDL). This has allowed modifications to be made and enhancements made to the system with simple changes to the microcontroller code.

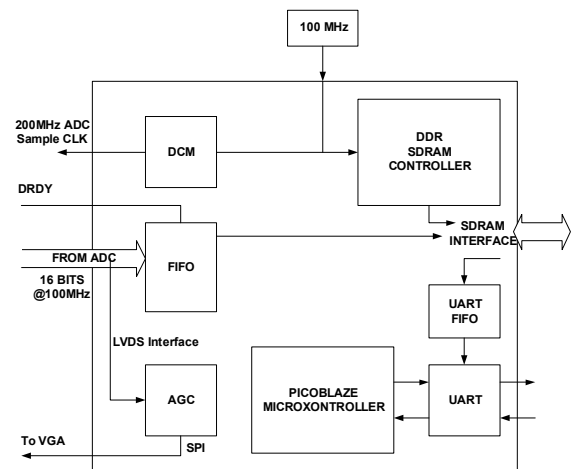


Figure 9: FPGA High Level Block Diagram

Figure 10 shows the designed RF front end PCB (top board), the high-speed ADC converter PCB (middle

board) and the digital controller PCB (bottom board), stacked to form the complete receiver structure.

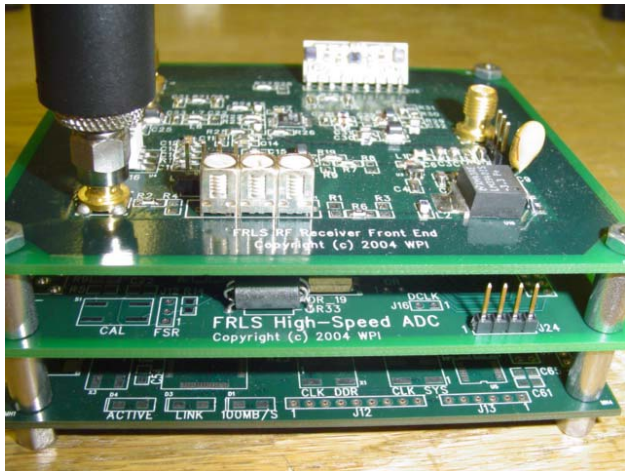


Figure 10: Designed Receiver Stack

TRANSMITTER FRONT END DESIGN AND DEVELOPMENT

The MC-UWB transmitter consists of three major system blocks. These include the digital back end, the digital to analog converter and the RF front end. The prototype transmitter currently consists of various evaluation boards which will be later implemented on a three PCBs in a similar configuration as the receiver. The high level block diagram of the RF front end is shown in Figure 11.

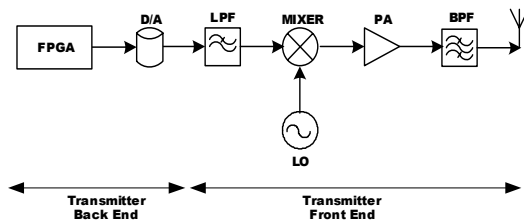


Figure 11: MC-UWB Transmitter

The transmitter front end consists of Low Pass Filter, Up-converting Mixer, Power Amplifier and Band Pass Filter. The Low Pass Filter used is a 7th order LC low pass filter similar to the one used in the receiver RF front end. These LPF have advantages of the LC design, that is, low insertion loss and high power handling. A high performance active mixer is used in up-converting mode. The mixer used has wide bandwidth on all its ports and very low intermodulation distortion. The mixer used in the transmitter is also suitable for high intercept applications. The required local oscillator signal to drive the mixers should be between -12 dBm and -3 dBm. An RF PLL frequency synthesizer similar to that being used in the receiver is used to generate the required mixer local

oscillator signal. A complete phase locked loop (PLL) is implemented on the bottom layer of the transmitter PCB by using the synthesizer with a loop filter and a suitable voltage controlled oscillator. The crystal oscillator used in the PLL implementation is a 10MHz reference frequency. The power amplifier chosen is capable of generating up to 2W CW output power and has a gain of 33dB. The frequency range of the power amplifier is 400 to 500 MHz. The correct matching network values were designed and the PA evaluation board was tuned as required. Band Pass Filter used is a triple tuned helical BPF similar to that used in receiver PCB. The designed transmitter RF front end PCB is shown in Figure 12.

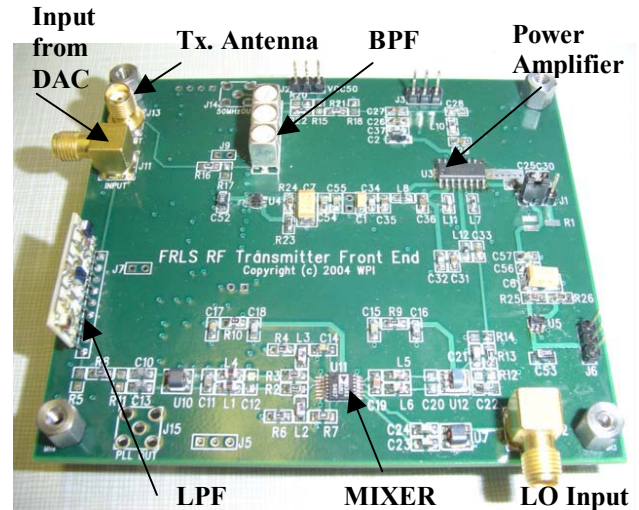


Figure 12: Designed Tx Front End PCB

TRANSMITTER BACK END DESIGN AND DEVELOPMENT

The digital back end uses the same digital controller board as used for the receiver digital back-end and described in an earlier section. The only hardware difference is in the removal of the termination resistors on the LVDS interface lines and replacement of the receiver functions with transmitter functional blocks. The transmitter operation is simpler than the receiver in that it only needs to transmit the OFDM symbols. Due to their relatively small size (currently 8192 samples) these symbols do not need to be stored and retrieved from the SDRAM and so can be loaded into BLOCK RAM in the FPGA and sent as part of the configuration bit stream to the FPGA.

Figure 13 shows the detailed block diagram of the digital back end of the receiver:

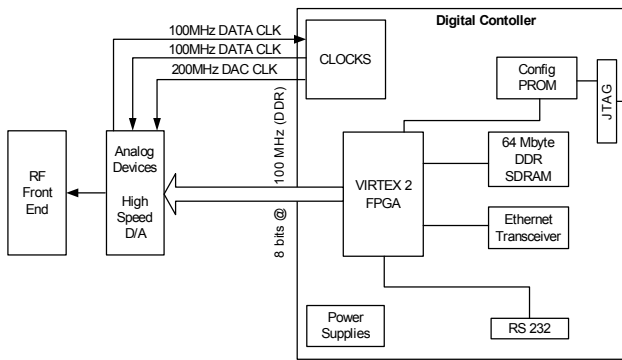


Figure 13: Detailed Receiver Back End Block Diagram

An Analog Devices AD9736 high-speed DAC is used for the DAC converter. It has 14-bit resolution and a maximum sample rate of 1.2 GSps. We are currently just using 8-bits, but the full 14-bits remain available through the LVDS interface to the FPGA. The interface consists of 14 pairs of differential data, and 3 differential pairs of clock signals. The output of the DAC is the input to the transmitter RF front end. All the necessary clocks and LVDS signals required by the converter are generated by the FPGA. A 100 MHz system clock is multiplied by a DCM to become a 200 MHz clock for input to the DAC. This clock becomes the sample clock for the DAC. The DAC returns this clock back to the FPGA, divided by 2, for use as a data clock. The data is driven onto the LVDS bus at double data rate.

Another function required on the transmitter digital controller board was an SPI interface to program the receiver and transmitter PLL. This is required to configure the local oscillator for upconversion and downconversion.

MC-UWB BASED RADIO TEST PLATFORM

The MC-UWB transmitter and receiver test platform uses the transmitter and the receiver front end and back end PCB designs that are discussed in the previous sections. Table 3 lists the test conditions for the MC-UWB system to be used for distance estimation.

Table 3: MC-UWB Based Distance Estimation Test Conditions

Radio Architecture	Direct Downconversion
System Setup	1 Transmitter – 1 Receiver (will be extended to multiple Tx-Rx)
Carrier Frequency	440 MHz
Signal Bandwidth	12.2 MHz
TCXO Stability	< 2.5 ppm
Transmitter Power	-15dBm to 15dBm
Transmitter DAC	8 bits at 200 MHz

Receiver adjustable gain control range	-11 dB to 35 dB
Receiver Noise Figure	5.7 dB
Receiver Sensitivity	-90 dBm
Receiver ADC	8 bits at 200 MHz
LO phase noise	-86.6 dBc/Hz

Figure 14 shows the high level block diagram of the test setup. The N data points that form the MC-UWB signal are loaded in to the digital controller board of the transmitter. The output of the digital Controller is the input of the DAC. This output is then the input to the RF analog front end board where the MC-UWB signal is upconverted, amplified and transmitted. Initially the tests were done in a controlled environment and thus the output of the transmitter is connected to the input of the receiver using RF cables of various increasing length l_i , thus artificially introducing delays in the received signal for longer cables. This received signal is then downconverted in the receiver RF board digitized using the ADC board and stored in the designed digital controller board.

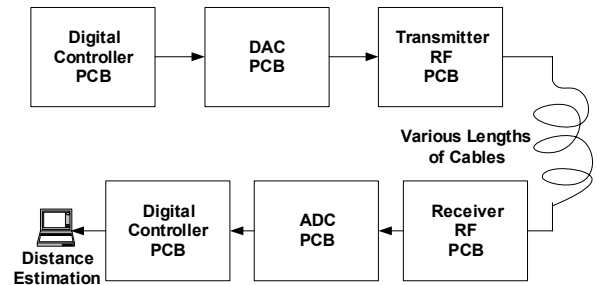


Figure 14: MC-UWB Based Distance Estimation Test Setup

The data stored by the digital controller PCB is transferred to the laptop for distance estimation. The length of the cable is the true distance between the transmitter and the receiver. Thus the results of the distance estimation should be close to the length of the cable. Five cables of various increasing lengths were used as the receiver was receiving the signal, making it look as the receiver and transmitter were being moved further apart. The results of the distance estimates are as shown in Figure 15. After increasing the cable length, each time five OFDM symbols were captured, which correspond to the sets of five points close to each other as seen in Figure 15. Five different cable lengths were used and hence a total of 25 OFDM symbols were captured. We can see that the distance estimates look like the expected staircase, where the jump in the step is the difference in the successive cable lengths.

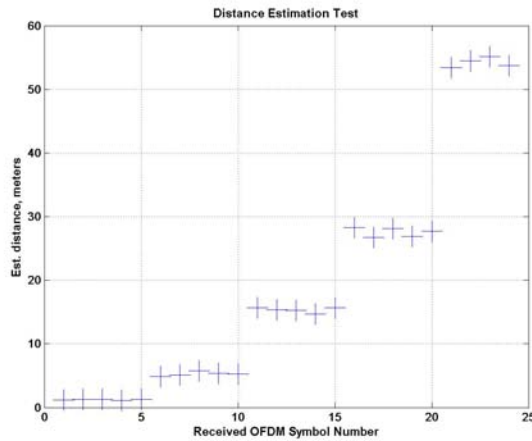


Figure 15: Distance Estimates for MC-UWB Based System

The distance estimate results shown in above figure are summarized in Table 4. The sources of errors are being further investigated. It can be seen that with the MC-UWB system and algorithms being designed and developed for precise position location, it is capable of estimating the distances within accuracy of one meter.

Table 4: Distance Estimates

l_i	Calibrated vacuum Cable Length (m)	Estimated Distance (m)	Error (m)
$i = 1$	1.2	1.5	0.3
$i = 2$	4.2	5	0.8
$i = 3$	17	16	1
$i = 4$	27.8	27	0.8
$i = 5$	51.5	53	1.5

CONCLUSIONS

In this paper we have described the design of a transmitter and the receiver that can be used for precise position location systems. The MC-UWB system that can be used for super resolution position estimation was designed and successfully tested. The custom made PCB designs include, receiver RF front end PCB, the ADC PCB and the Digital controller PCB to form a portable receiver stack. The transmitter RF front end PCB design was also discussed. The designed receiver stack is suitable for systems that use Multi Carrier, wide band signal structure. The results discussed in the paper show that using the proposed MC-UWB system distance estimate of accuracy within one meter can be achieved.

Currently multiple stacks of the proposed receiver structure are being built to expand the test setup to multiple receiver system. This will lead to real time wireless tracking of the transmitter using TDOA technique.

ACKNOWLEDGMENTS

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